IN THE SPECIFICATION:

Please replace paragraph 0004 with the following paragraph:

[0004] FIG. 1 is a block diagram illustrating a general digital TV receiver having such symbol clock recovery. Referring to FIG. 1, if a radio frequency (RF) signal modulated in a VSB mode is received through an antenna 101, a tuner 102 selects a desired channel frequency. Then, the tuner 102 converts a VSB signal of an RF band inserted in the channel frequency to a first intermediate frequency (IF) band, and outputs to an analog processor 103. The analog processor 103 performs passband filtering and gain controlling to the first IF signal outputted from the tuner 102 for converting the first IF signal into a second IF signal, and outputs to an A/D (Analog/Digital) converter 104. The A/D converter 104 digitizes and outputs the second IF signal to a phase splitter 105.

Please replace paragraph 0007 with the following paragraph:

[0007] FIG. 2 is a block diagram of a conventional structure of the carrier recovery 106 employing a FPLL (Frequency Phase Locked Loop). That is, the carrier recovery ~~108~~106 having the FPLL demodulates the I and Q passband signals outputted from the A/D converter ~~105~~104 into the baseband I and Q signals for frequency and phase locking.

Please replace paragraph 0008 with the following paragraph:

[0008] Referring to FIG.2, the passband I and Q signals being digitized through the A/D converter 104 and the phase splitter 105 are inputted to a complex multiplier 201 of the carrier recovery. At this time, the real signal (r(t)) and the imaginary signal (~~q~~i(t)) outputted from the

phase splitter 105 is expressed as a following formula.

Please replace paragraph 0011 with the following paragraph:

[0011] Meanwhile, the complex multiplier 201 of the carrier recovery 106 multiplies the passband ~~I~~r(t) and ~~Q~~i(t) signals as the formula 1 by a standard carrier signals NCO (Number Controlled Oscillator) I and NCOQ outputted from the NCO 205, and converts the passband ~~I~~r(t) and ~~Q~~i(t) signal into the baseband I and Q signals (I'(t), Q'(t)) as a following formula 2.

Please replace paragraph 0014 with the following paragraph:

[0014] The I and Q signals [I'(t), Q'(t)] of the baseband are outputted to a low pass filter 202 as well as to the symbol clock recovery 107 and the digital processor 108.

Please replace paragraph 0015 with the following paragraph:

[0015] The low pass filter 202 filters the ~~low pass~~ I'(t) and Q'(t) signals to detect the carrier and outputs to an error detector 203. That is, the carrier recovery 106 recovering the carrier needs only signals around the frequency having the pilot frequency in a band width of 6 MHz and, therefore, the low pass filter 202 prevents the efficiency of the carrier recovery from being reduced by removing the remaining frequency component having data component from the I'(t) and Q'(t) signals.

Please replace paragraph 0020 with the following paragraph:

[0020] However, if the carrier recovery is not completely carried out in the carrier recovery 106, the symbol clock recovery 107 recovers the symbol clock from the signal of the formula 2.

Thus, the symbol clock recovery 107 is not normally performed being influenced by the frequency and the phase between the carrier signals employed by the receiver and the standard carrier signal generated from the receiver such as Δwc and Ψ.

Please replace paragraph 0026 with the following paragraph:

[0026] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the digital TV receiver includes an A/D converter for converting an analog signal into a digital signal, a carrier recovery for converting the digital passband signal into a digital baseband signal, and a symbol clock recovery for converting digital baseband real/imaginary component signals into OQAM (Offset Quadrature Amplitude Modulation) type of real/imaginary component signals, detecting timing error information by high-passband-filtering, squaring, and adding the OQAM real/imaginary signals, and for generating and outputting at least two times the frequency of the symbol clock corrected from the detected timing error information.

Please replace paragraph 0030 with the following paragraph:

[0030] The OQAM converter multiplies digital baseband real/imaginary component signals interpolated and outputted from the resampler by a fixed frequency with a center frequency of 2.690559_MHz for converting digital baseband real/imaginary component signals into the OQAM real/imaginary component signals.

Please replace paragraph 0031 with the following paragraph:

[0031] The symbol clock recovery includes an OQAM converter for converting each of the

digital baseband real/imaginary signals outputted from the carrier recovery into OQAM real/imaginary component signals; a high pass filter performing a high-passband-filtering to the OQAM real/imaginary component signals outputted from the OQAM converter for removing information of data section; a squarer for squaring each of the OQAM real/imaginary component signals filtered by and outputted from the high passband filter, and adding and outputting the calculation; a pre-filter for passing only a frequency of a particular band to recover the symbol clock from the output of the squarer; a timing error detector for detecting timing error information from the output of the pre-filter; a filtering member for filtering only the low passband signal from the timing error information outputted from the timing error detector; and ~~an~~ variable oscillator ~~NCO~~ for generating at least two times the frequency of the symbol clock recovered according to low passband signals of the filtered timing error information and outputting to the ~~first resampler~~A/D converter.

Please replace paragraph 0032 with the following paragraph:

[0032] The OQAM converter multiplies the VSB digital baseband real/imaginary component signals outputted from the carrier recovery by the fixed frequency with the center frequency of 2.690559 MHz for converting the VSB digital baseband real/imaginary component signals into the OQAM real/imaginary component signals.

Please replace paragraph 0042 with the following paragraph:

[0042] The symbol clock recovery 400 includes an OQAM converter 401 for converting VSB transmitting type of real/imaginary component signals (VSB I and VSB Q) outputted from a resampler ~~201~~206 into OQAM transmitting type of real/imaginary component signals(OQAM I

and OQAM Q), a high pass filter 402 for high-passband-filtering each of the I and Q component signals (OQAM I and OQAM Q), a first squarer 403 for squaring the OQAM real component signal (OQAM I) outputted from the high pass filter ~~403~~402, a second squarer 404 for squaring the OQAM imaginary component signal (OQAM Q), and adder 405 for adding an output of the first squarer 403 to the output of the second squarer 404, a pre-filter 406 for passing an edge part of the output spectrum of the adder 405, a Gardner phase error detector 407 for outputting timing error information from the signal passed through the pre-filter 406, a ~~loop~~low pass filter 408 for filter a low passband signal component from the timing error information outputted from the Gardner phase error detector 407, an NCO 409 for converting the output frequency in accordance with the low passband component of the timing error information and controlling the sampling timing of the resampler ~~201~~206.

Please replace paragraph 0043 with the following paragraph:

[0043] The first embodiment composed as abovementioned shows a case that the A/D converter 104 samples a second IF signal at the fixed frequency, which is~~i.e., the fixed frequency~~ different from the symbol clock frequency~~,~~ and normally ~~at~~ 25 MHz, generated from the fixed oscillator 207 so as to digitalize the signal. In other words, although data sampled at ~~25~~21.52 MHz which is at least two times the frequency of the symbol clock is transmitted at the transmitter, data outputted from the A/D converter 104 is digital data sampled at 25 MHz.

Please replace paragraph 0044 with the following paragraph:

[0044] In this case, the fixed frequency oscillated in the fixed oscillator ~~202~~207 is higher than at least two times the frequency of the symbol clock. Since the data rate is different and

there is a difficulty in controlling, the resampler ~~201~~206 is arranged between the carrier recovery 106 and the symbol clock recovery 400.

Please replace paragraph 0045 with the following paragraph:

[0045] The resampler ~~201~~206 samples the digital baseband signal at the two times the frequency of the symbol clock, i.e., 21.-52_MHz, so as to output the signal for recovering the symbol clock.

Please replace paragraph 0046 with the following paragraph:

[0046] The resample ~~201~~206 performs a role of changing the sampling rate. In other words, the data sampled at 21.-52_MHz and received is sampled at 25_MHz by the A/D converter 104 and outputted. The resampler ~~201~~206 resamples the data to at least two times the frequency of the symbol clock, i.e., 21. 52_MHz and outputs the data.

Please replace paragraph 0047 with the following paragraph:

[0047] For this, the resampler ~~201~~206 interpolates the baseband digital signal passed through and outputted from the A/D converter 104 and the carrier recovery 106 into the ~~synchronized~~ digital signal synchronized at the at least two times the frequency 2fs of the symbol clock by employing the output frequency of the symbol clock recovery 400. The interpolated signals are outputted to the symbol clock recovery 107 as well as to a digital processor 108 for performing channel lighting, phase tracking, and an error correcting.

Please replace paragraph 0048 with the following paragraph:

[0048] The symbol clock recovery 400 obtains the timing error of the current symbol clock and generates the frequency proportion to the timing error so as to output the frequency to the resampler ~~201~~206.

Please replace paragraph 0049 with the following paragraph:

[0049] The OQAM converter 401 of the symbol clock recovery 400 multiplies VSB I and Q signals resampled at 21.~~-~~52_MHz and outputted from the resampler ~~201~~206 by the fixed oscillating frequency with a center frequency for converting the baseband VSB I and Q signals into OQAM I and Q signals, and outputs the signals to the high pass filter 402.

Please replace paragraph 0050 with the following paragraph:

[0050] FIGS. 4A to ~~5~~4D illustrated a frequency spectrum for the real component signal. FIG. 4A illustrates a VSB baseband I signal inputted to the OQAM converter 401 and FIG. 4B illustrates an OQAM I signal outputted from the OQAM converter 401. FIG. 4C is a frequency characteristic of the high pass filter 402, and FIG. 4D illustrates an OQAM I signal having a frequency characteristic and passed through the high pass filter 402. In other words, the high pass filter 402 removes information of the data section from the OQAM I and Q signals and outputs the signals to the first squarer 403 and second squarer 404.

Please replace paragraph 0052 with the following paragraph:

[0052] The pre-filter 406 passes only the edge portion of the spectrum for obtaining the timing error information from the signal outputted from the adder 405, and outputs the signal to the Gardner phase error detector 407. The Gardner phase error detector 407 multiplies a difference

between two symbol samples by one of middle sample values so as to obtain the timing error information and outputs the signal to the loop-filter 408. The loop-filter 408 filter only low passband signal component from the timing error information detected from the Gardner phase error detector 407 and outputs the component to the NCO 409. The NCO 409 converts the output frequency in accordance with the low passband component of the timing error information so as to control the sampling timing of the resampler ~~201~~206.

Please replace paragraph 0054 with the following paragraph:

[0054] In this case, an output of the loop filter ~~608~~408 low passband filtering the timing error information of the current symbol detected from the symbol clock recovery 600 is inputted to a variable oscillator 609 newly generating at least two times the frequency of the symbol clock. The variable oscillator 609 newly generates at least two times the frequency of the symbol clock from the low passband filtered timing error information so as to output to the A/D converter 104.

Please replace paragraph 0055 with the following paragraph:

[0055] In this instance, the OQAM converter is not necessary at all when there is no high pass filter at the symbol clock recovery in the first and second embodiments of the present invention because outputs of the two squarers and the adder are converted into a signal in FIG. 3 even if an input signal is not the baseband signal. However, when the high pass filter is employed at a front end of the two squarers, most of frequency areas with the data are removed, and only the component needed for the symbol clock recovery is inputted to the squarers so as to improve the remained jitter characteristic of the symbol clock recovery. When there is a heavy noise in the transmitting channel owing to a multi-passage, an efficiency of the symbol clock

recovery is increased because the symbol clock recovery is not interfered by the movement of data. The present invention may be applied to all ATSC types of digital broadcasting receiver employing the VSB modulation.